Test Method to Evaluate High-g Component Susceptibility

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Daniel Peairs, Nathan Millard, Triet Dao, Marc Worthington
L3 Defense Electronic Systems

Ericka Amborn, Frank Marso, Craig Doolittle

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L3 Defense Electronic Systems (L3 DES)

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Introduction

• Fuze level testing under severe loading conditions:
  – Expensive
  – May not identify risk early in design process
  – Difficult to pinpoint cause of fuze level failures
  – Components may function normally post-test despite intra-test failure

The test methodology discussed here allows for a single electronic component to be tested and actively monitored during a shock event.
ESAD Electronics Characterization and Survivability

• Single Hopkinson Bar Testing
  – Conduct high acceleration/high frequency testing of select electronic components

• Modeling of components and FEA
  – Correlate high fidelity FEA models of components with empirical results
Test Set Up

• Single Hopkinson Bar
  – Steel Striker
  – Steel Bar
  – Threaded interface for tip
  – PCB mounted to tip with single component
  – Strain gauges
  – Laser vibrometer

Figure 3. General Test Layout
Test Overview

• Single Hopkinson Bar testing included 3 each of 8 different components commonly used in L3 DES designs

• Tested at 3 different acceleration severity levels
  – System capable of producing pulses ranging from 1000 g’s to over 250,000 g’s

• Each component tested in an axial and 2 lateral configurations
Downselected Component List

- Selected based on size, availability or previous history in survivable firesets

<table>
<thead>
<tr>
<th>Component Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator</td>
<td>Oscillator 1 - Delay block</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Oscillator 2 - Oscillator for logic timing</td>
</tr>
<tr>
<td>Complex Logic</td>
<td>Complex Logic 1 - Leaded microcontroller</td>
</tr>
<tr>
<td>Complex Logic</td>
<td>Complex Logic 2 - Bottom terminated microcontroller</td>
</tr>
<tr>
<td>Complex Logic</td>
<td>Complex Logic 3 - FPGA</td>
</tr>
<tr>
<td>Discrete Logic</td>
<td>Schmitt Trigger</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Capacitor 1 - Tantalum capacitor</td>
</tr>
<tr>
<td>Capacitor</td>
<td>Capacitor 2 - Ceramic capacitor</td>
</tr>
</tbody>
</table>
### Test Methodology

- A set of inputs was selected for each individual component in this test. The expected behavior of each component was characterized and recorded before, during, and after each test. Any change in the output was evaluated and analyzed using the appropriate failure analysis method.

- The output data was correlated against the strain gage derived acceleration.

<table>
<thead>
<tr>
<th>Component</th>
<th>Input</th>
<th>Expected Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator 2</td>
<td>5V, GND</td>
<td>8MHz Output</td>
</tr>
<tr>
<td>Schmitt Trigger</td>
<td>5V, GND, 100kHz, 50% duty cycle, 0-5V</td>
<td>Inversion of the input</td>
</tr>
<tr>
<td>Oscillator 1</td>
<td>3.3V, GND, 50 kHz, 75% duty cycle, 0-3.3V</td>
<td>Output rises 10us after input is enabled. Falls when input is falling.</td>
</tr>
</tbody>
</table>
| Complex Logic 1  | 3.3V, GND                    | Nominal: 50kHz, 50% duty cycle
Reset: 75kHz, 50% duty cycle for ~100us before resuming normal operation |
| Complex Logic 2  | 3.3V, GND                    | Nominal: 100kHz, 50% duty cycle
Reset: 200kHz, 50% duty cycle for ~100us before resuming normal operation |
| Complex Logic 3  | 3.3V, 2.5V, GND, Negative reset, 8MHz clock | Nominal: 125kHz, 50% duty cycle
Reset: 500kHz, 50% duty cycle for ~100us before resuming normal operation |
| Tantalum Capacitor | 19kHz, 20% duty cycle, 0-5V | RC charging triangular waveform from 0V to around 3.2V depending on capacitance |
| Ceramic Capacitor | 800Hz, 20% duty cycle, 0-5V | RC charging triangular waveform from 0V to around 3.2V depending on capacitance |
Test Setup

- High speed camera
- UUT
- Support circuit
- Laser vibrometer protection

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## Results Summary

<table>
<thead>
<tr>
<th>Type</th>
<th>Component</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillators</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Complex Logic 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Complex Logic / Discrete Logic</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitors</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Key

<table>
<thead>
<tr>
<th>Measured Test Severity</th>
<th>Unaffected</th>
<th>Affected During Test</th>
<th>Affected Post Test</th>
<th>Part Failed</th>
<th>Test Not Conducted Due to Previous Failure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Image from ARA*
Oscillator 1 – Axial Impact at Severity Level 3

- Delays both greater and smaller than the expected 10us can be observed in the above figure.
- In the current setup for a 10us delay, a delay shift as great as ~70% can be observed in an individual pulse. It’s unlikely this delay shift would scale in a 10ms set up.
- Further testing is required to verify this claim.
Oscillator 1 – Lateral Y at Severity Level 3

- Missing pulses indicate component malfunction
- Component showed a small, permanent increase in on-time pulse width after the test
Oscillator 1 – Post Test Imaging

• Pre and post-test high resolution x-rays were conducted on all components

• Internal bond wires appear to be intact

• CT Scans also conducted to better understand internal geometries
Ceramic Capacitor – Axial at Severity Level 3
Ceramic Capacitor – Axial at Severity Level 3

- 42% decrease in capacitance was observed
- High resolution x-rays were not able to identify damage within capacitor layers

<table>
<thead>
<tr>
<th></th>
<th>Computed Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
</tr>
<tr>
<td>Pre-Test</td>
<td>105.57</td>
</tr>
<tr>
<td>Test</td>
<td>55.70</td>
</tr>
<tr>
<td>Post-Test</td>
<td>61.17</td>
</tr>
</tbody>
</table>
Component Testing Summary

- Developed enhanced methodology for assessing component susceptibility to high shock environments
- Evaluated several classes of components commonly used in ESADs
- Actively monitored single components during a shock event
  - Permits assessment of risk during High-g events that is not possible with pre and post test interrogation only
Acknowledgements

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