High Reliability FPGAs in Fuze and Fuze Safety Applications

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Agenda

- Why use FPGAs in Fuze applications
- Antifuse FPGAs in Fuze and Fuze safety systems
  - Heritage and Outlook
- Flash FPGAs – considerations for Fuze Safety and Arming
  - Architecture and Programming
  - Reliability, Retention, Qualification
  - Radiation
  - Power consumption
  - Heritage and Outlook
- Conclusion
Why FPGAs in Fuze and Safety Applications

- Many reasons to use FPGAs for integration of logic circuits in fuze safety and arming systems
  - Cost effective
    - No non-recurring engineering cost, unlike custom circuits (ASICs)
  - High levels of integration
    - Fuze safety and arming circuits can easily be integrated into modern FPGAs
  - Small form factor
    - Flat pack and fine ball grid array packages
  - High reliability
    - Millions of units shipped, extensive reliability data, various screening levels
  - Low power consumption
    - For battery-powered equipment, or thermally-constrained environments

3mm x 3mm CS81 Package
Antifuse FPGAs in Fuze applications

- Microsemi antifuse FPGAs have a long heritage in fuze applications.
Microsemi has a policy of long term production
• We hold many years of wafer stock after fab production has ended
• 12 month last time buy, plus 6 month shipment window after final order

Now is the time to start thinking about Flash FPGA technology for next generation fuze safety and arming systems
Flash FPGAs
Considerations for Fuze Safety and Arming
Introduction to Flash FPGAs

- Microsemi has a 20 year legacy in Flash FPGAs
  - ProASIC 0.25um
  - ProASIC Plus 0.22um
  - ProASIC3 and derivatives 130nm
    - Igloo (low power FPGA), Fusion (FPGA + mixed signal), SmartFusion (FPGA + embedded MCU)
  - Igloo2, SmartFusion2 (FPGA + embedded MCU) 65nm
  - Next generation in development

- This presentation focuses on reliability studies and qualification data for the 130nm and 65nm Flash FPGA product lines
  - Current generation, 65nm (Igloo2, SmartFusion2)
  - Preceding generation, 130nm (ProASIC3, Igloo, Fusion, SmartFusion)

- Flash FPGA qualification heritage
  - ProASIC Plus (0.22u) qualified to MIL-STD-883B in 2005
  - ProASIC3 (130nm) was qualified to MIL-STD-883B in 2010
  - ProASIC3 (130nm) was qualified to QML class Q in 2015
  - Igloo2 and SmartFusion2 (65nm) were qualified to JEDEC JESD22 in 2013
Architectural Overview of Flash FPGAs

- All generations of Microsemi terrestrial Flash FPGAs have similar interconnect architecture
  - Device personality is determined by the connection of routing tracks
  - Switch transistor with floating gate connects or disconnects routing tracks
  - Non-volatile floating gate determines state of switch transistor – on or off

Switch Transistor Determines Whether Routing Tracks are Connected or Disconnected
Flash Cell Architecture

- In Microsemi Flash-based FPGAs, each switch transistor is accompanied by a sense transistor which shares the same floating gate and control gate.
- The sense transistor is used for programming, erasing, and margining.

\[ V = \frac{Q}{C_T} + \sum_{k=1}^{K} \frac{C_k}{C_T} V_k \]

\[ C_T = C_{CG} + C_D + C_S + C_{SUB} \]
Advantages of Flash FPGA Switch

- Flash FPGAs are better suited to Fuze applications than SRAM FPGAs
  - Significantly more compact – smaller package size
  - Lower power consumption
  - Non volatile – requires no external design storage device
  - Non volatile – live at power-up
  - Immune to radiation-induced upsets
ProASIC3 Basic Logic Cell (130nm)

- ProASIC3 Logic Cell implements any 3-input combinatorial logic function or a D-type Flip Flop with enable

Each logic cell is equivalent to 1 to 8 ASIC gates
Igloo2 / SmartFusion2 Logic Cell (65nm)

- A fully permutable 4-input LUT
- A dedicated carry chain based on the carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT
Physics of Program and Erase

- **Programming**
  - Electrons injected into the floating gate
  - Floating gate becomes negatively charged
  - Switch is held in “Off” state

- **Erasing**
  - Electrons pushed out of the floating gate
  - Floating gate becomes positively charged
  - Switch is held in “On” state
What is Margining?

- What is margining?
  - Margining is the operation for determining the amount of charge in the flash cell

- Why do we need it?
  - In order to do any flash reliability studies, the ability to accurately track the amount of charge in a floating gate is essential

- One of the unique features of Microsemi Flash FPGAs is the ability to margin all flash cells in the FPGA fabric even after the part has been packaged
How Margining Works

- All cells are unselected to measure the leakage of the sense devices prior to margining.

- $V_{CG}$ is swept until a specific amount of current ($I_{SENSE}$) passes through the sense device based on the voltage ($V_{SENSE}$) on the column line.
  - $V_{SENSE}$ & $I_{SENSE}$ is a reference value for defining the margined voltage of a cell.
Margining Results

- Typical margin distribution curve

<table>
<thead>
<tr>
<th>Erase Margin</th>
<th>Program Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON State</td>
<td>OFF State</td>
</tr>
<tr>
<td>Increase (R_{\text{ON}}) for Erased Cell</td>
<td>Decrease (R_{\text{ON}}) for Programmed Cell</td>
</tr>
</tbody>
</table>

- Erased cells are in negative region
  - \(V_{\text{FG}}\) (uncoupled) = 1V (sense device ON)
  - Goal: Turn sense device OFF (increase \(R_{\text{ON}}\)) until \(I_{\text{SENSE}}\) is reached
  - Negative margined voltage

- Programmed cells are in positive region
  - \(V_{\text{FG}}\) (uncoupled) = -1.5V (sense device OFF)
  - Goal: Turn sense device ON (decrease \(R_{\text{ON}}\)) until \(I_{\text{SENSE}}\) is reached
  - Positive margined voltage
Reliability Studies – HTR (High Temp Retention)

- Charges in a floating gate can leak away
  - This natural phenomenon can cause a programmed cell to become un-programmed (or an erased cell to become un-erased) in the most extreme case
  - The ability of a flash switch to maintain its charge (retention) will affect the performance/functionality of a device

- Microsemi performed HTR with a 225°C unbiased bake for 3,000 hrs (cumulative)
  - Equivalent to 23 years operation life @ 110°C junction using $E_a = 0.6\text{eV}$

![PROGRAM RETENTION](image1)

![ERASE RETENTION](image2)
Reliability Studies – Endurance

- **Endurance**
  - Multiple program/erase cycles can cause degradation to the NVM cell
    - Charges get trapped by the oxide as they tunnel through during program/erase, this reduces the amount of charges that can be stored in the floating gate
  - Microsemi performed endurance at 25°C for 500 program/erase cycles with 100% pattern
Reliability Studies – HCI (Hot Carrier Injection)

- HCI occurs when electrons get enough energy from the lateral and vertical field
  - Lateral field is dependent on \( V_{DS} \)
  - Vertical field is dependent on \( V_{GS} \)
- HCI is a mechanism used for writing flash cells
  - Unintended HCI will cause functional issue

\[
V_D - V_S = V_{DS}
\]

With higher \( C_D \) loading, the \( V_{DS} \) will be reduced
--- \( V_D \) with a balance loading

Simulations for all situations are performed to determine the \( V_{DS} \)
- The data collected is used to set rules for the Place & Route algorithm
- Electrons must attain 3.2eV to get into the conduction band hence this is less of a concern for 130nm and 65nm Flash FPGAs relative to older generations
# ProASIC Plus (0.22um) Flash FPGA MIL-STD-883B Qualification Summary

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Test Condition</th>
<th>No. of Qual Lots</th>
<th># Failures / Sample Size</th>
<th>Test Duration Pull Point</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Group A</strong></td>
<td>$T_A = -55^\circ \text{C to } 125^\circ \text{C}$, $V_{DD} = 2.3 \text{V to } 2.7 \text{V}$, $V_{DDP} = 3 \text{V to } 3.6 \text{V}$, $V_{PP} = V_{DD}$, $V_{PN} = \text{GND}$ (Mil-Std-883, TM 5005)</td>
<td>1</td>
<td>0/129 (+3 spares)</td>
<td>NA</td>
<td>PASSED</td>
</tr>
<tr>
<td><strong>Group C</strong></td>
<td>$T_A = 150^\circ \text{C}, T_J = 160^\circ \text{C}$ $V_{DD} = 2.7 \text{V}$, $V_{DDP} = 3.6 \text{V}$, $V_{PP} = 16.2 \text{V}$, $V_{PN} = -13.6 \text{V}$ (Mil-Std-883, TM 5005)</td>
<td>1</td>
<td>0/129 (+3 spares)</td>
<td>184hrs (no pull point in between)$^1$</td>
<td>PASSED</td>
</tr>
<tr>
<td><strong>Group D3/D4</strong></td>
<td>-65$^\circ$C to 150$^\circ$C (Mil-Std-883, TM 5005)</td>
<td>1</td>
<td>0/15, 0/15</td>
<td>N/A</td>
<td>PASSED</td>
</tr>
<tr>
<td><strong>ESD</strong></td>
<td>Programmed (Mil-Std-883, TM3015)</td>
<td>1</td>
<td>0/3 (HBM)</td>
<td>N/A</td>
<td>PASSED 1800V</td>
</tr>
<tr>
<td><strong>Capacitance</strong></td>
<td>(Mil-Std-883, TM3012)</td>
<td>1</td>
<td>0/3</td>
<td>N/A</td>
<td>PASSED</td>
</tr>
<tr>
<td><strong>Latchup</strong></td>
<td>(JESD-78)</td>
<td>1</td>
<td>0/3</td>
<td>N/A</td>
<td>PASSED</td>
</tr>
</tbody>
</table>

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Note 1: As an engineering study, additional 500 hours of HTOL at 125$^\circ$C was performed on the Group C lot. No failure was observed.
ProASIC3 (130nm) Flash FPGA
MIL-STD-883B Qualification Summary

<table>
<thead>
<tr>
<th>Qualification #</th>
<th>M036</th>
<th>DATE: 03/30/2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qualification Description:</td>
<td>Military qualification of RT3PEL (600 / 3000) per MIL-STD-883B</td>
<td></td>
</tr>
<tr>
<td>Qualification Vehicle:</td>
<td>RT3PE3000L</td>
<td>Package:</td>
</tr>
<tr>
<td>Wafer lot number:</td>
<td>QHR8G</td>
<td>Date Code:</td>
</tr>
<tr>
<td>MESA Lot Number:</td>
<td>62941039</td>
<td>Fab:</td>
</tr>
<tr>
<td>PCN Required?:</td>
<td>N/A</td>
<td>PCN#:</td>
</tr>
</tbody>
</table>

Qualification Results & Conclusion:
- The RT3PEL qualification devices have passed all requirements specified in the Qualification Proposal.
- Therefore, RT3PEL MIL-STD-883B is hereby qualified and is ready to be released for production.

### Qualification Results Summary

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Test Condition</th>
<th>No. of Qual Lots</th>
<th># Failures / Sample Size</th>
<th>Test Duration Pull Point</th>
<th>Failure Analysis Results/Mechanism</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group C (TM 5005, Table III)</td>
<td>$T_A = 125^\circ$C, $Vcc / Vccpill = 1.575V$, $Vcc/VMV / Vjtag = 3.6V$,</td>
<td>1</td>
<td>0/79 (+2 Spares)</td>
<td>168 hrs ($1^{st}$) 500 hrs ($2^{nd}$) 1000 hrs (final)</td>
<td>PASSED$^1$</td>
</tr>
<tr>
<td>Group D3/D4 (TM 5005, Table IV)</td>
<td>$-65^\circ$C to 150$^\circ$C</td>
<td>1</td>
<td>0/15</td>
<td>100 cycles</td>
<td>PASSED</td>
</tr>
<tr>
<td>ESD (TM3015)</td>
<td></td>
<td>1</td>
<td>3 (HBM)</td>
<td></td>
<td>PASSED$^2$</td>
</tr>
<tr>
<td>Capacitance (TM3012)</td>
<td></td>
<td>1</td>
<td>3</td>
<td></td>
<td>PASSED</td>
</tr>
<tr>
<td>Latchup (JESD-78)</td>
<td>$T_A = 125^\circ$C</td>
<td>1</td>
<td>6</td>
<td></td>
<td>PASSED</td>
</tr>
<tr>
<td>Characterization (RT3PE3000L)</td>
<td>$T_A = -55^\circ$C to 125$^\circ$C</td>
<td>1</td>
<td>5</td>
<td></td>
<td>PASSED</td>
</tr>
</tbody>
</table>
Flash FPGA Reliability Summary


### Reliability Summary

#### Table 1: Reliability Summary: FIT Rate by Device Technology

<table>
<thead>
<tr>
<th>Device Technology</th>
<th>Number of CMOS Failures</th>
<th>Device Hours</th>
<th>T_J (°C)</th>
<th>EA, eV</th>
<th>Confidence</th>
<th>FIT</th>
<th>MTTF</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 µm CMOS FPGA</td>
<td>1</td>
<td>3.60E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>5.62</td>
<td>1.78E+08</td>
</tr>
<tr>
<td>1.0 µm CMOS FPGA (RH1020)</td>
<td>0</td>
<td>3.97E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>23.05</td>
<td>4.34E+07</td>
</tr>
<tr>
<td>0.8 µm CMOS FPGA (RH1280)</td>
<td>1</td>
<td>9.16E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>22.04</td>
<td>4.54E+07</td>
</tr>
<tr>
<td>0.8 µm CMOS FPGA</td>
<td>0</td>
<td>2.05E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>4.47</td>
<td>2.24E+08</td>
</tr>
<tr>
<td>0.6 µm CMOS FPGA</td>
<td>0</td>
<td>1.82E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>5.04</td>
<td>1.99E+08</td>
</tr>
<tr>
<td>0.6 µm RT54SX CMOS FPGA</td>
<td>0</td>
<td>2.29E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>39.88</td>
<td>2.51E+07</td>
</tr>
<tr>
<td>0.45 µm CSM CMOS FPGA</td>
<td>1</td>
<td>1.09E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>18.05</td>
<td>5.41E+07</td>
</tr>
<tr>
<td>0.45 µm UMC CMOS FPGA</td>
<td>0</td>
<td>3.80E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>24.06</td>
<td>4.16E+07</td>
</tr>
<tr>
<td>0.35 µm CMOS FPGA</td>
<td>0</td>
<td>6.31E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>14.51</td>
<td>6.89E+07</td>
</tr>
<tr>
<td>0.25 µm MEC CMOS FPGA</td>
<td>2</td>
<td>7.51E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>41.40</td>
<td>2.42E+07</td>
</tr>
<tr>
<td>0.25 µm Infinion Flash CMOS FPGA</td>
<td>0</td>
<td>3.62E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>25.30</td>
<td>3.95E+07</td>
</tr>
<tr>
<td>0.25 µm UMC CMOS FPGA</td>
<td>0</td>
<td>7.84E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>1.17</td>
<td>8.57E+08</td>
</tr>
<tr>
<td>0.22 µm UMC CMOS FPGA</td>
<td>0</td>
<td>5.19E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>1.76</td>
<td>5.67E+08</td>
</tr>
<tr>
<td>0.22 µm UMC Flash CMOS FPGA</td>
<td>0</td>
<td>8.49E+07</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>10.77</td>
<td>9.28E+07</td>
</tr>
<tr>
<td>0.15 µm CMOS FPGA</td>
<td>2</td>
<td>4.56E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>6.82</td>
<td>1.47E+08</td>
</tr>
<tr>
<td>0.13 µm Infinion Flash CMOS FPGA</td>
<td>0</td>
<td>4.56E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>2.01</td>
<td>4.99E+08</td>
</tr>
<tr>
<td>0.13 µm UMC Flash CMOS FPGA</td>
<td>1</td>
<td>2.78E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>7.28</td>
<td>1.37E+08</td>
</tr>
<tr>
<td>0.085 µm UMC Flash CMOS FPGA</td>
<td>0</td>
<td>3.64E+08</td>
<td>55</td>
<td>0.7</td>
<td>60%</td>
<td>3.22</td>
<td>3.11E+08</td>
</tr>
</tbody>
</table>
No Configuration Failures Due To Radiation

- Immunity to configuration failures due to atmospheric neutron radiation
  - Increasing problem for SRAM-based FPGAs
- Microsemi’s Antifuse- and Flash-based FPGAs are immune

**Antifuse FPGAs**

- Antifuses have a permanently-programmed metallic link, which cannot be altered by energetic particles or other radiation.
- ![Diagram](image)

**Flash FPGAs**

- High energy particles (atmospheric neutrons, heavy ions in space) are unable to generate sufficient charge to cause the floating gate to erroneously change state.
- ![Diagram](image)

**SRAM FPGAs**

- Incoming neutron causes firm error in logic modules leading to
- ![Diagram](image)
- Incoming neutron causes firm error in routing matrix leading to
- ![Diagram](image)
Weapon Effect Radiation Testing

Microsemi FPGAs for Strategic Applications

<table>
<thead>
<tr>
<th></th>
<th>ProASIC3</th>
<th>Igloo</th>
<th>Igloo2</th>
<th>SmartFusion2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dose Rate (Upset, rad/sec)</td>
<td>1.4E+10</td>
<td></td>
<td>2.7E+09</td>
<td></td>
</tr>
<tr>
<td>Dose Rate (Survive, rad/sec)</td>
<td>&gt;7.8E+10</td>
<td>&gt;6.1E+10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Technology</td>
<td>130nm</td>
<td>Yes</td>
<td>65nm</td>
<td></td>
</tr>
<tr>
<td>Mil Temp Plastic</td>
<td>Yes</td>
<td></td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>Mil Temp Hermetic</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Max LE / FF</td>
<td>75K Tiles</td>
<td></td>
<td>146K</td>
<td></td>
</tr>
<tr>
<td>Max SRAM</td>
<td>500Kbits</td>
<td></td>
<td>4.5Mbits</td>
<td></td>
</tr>
<tr>
<td>Max Mathblocks</td>
<td>-</td>
<td></td>
<td>240</td>
<td></td>
</tr>
</tbody>
</table>

- Contact Microsemi for further information
  keno@microsemi.com
## Industry’s Lowest Power Consumption

<table>
<thead>
<tr>
<th>Feature</th>
<th>IGLOO nano</th>
<th>ProASIC3 nano</th>
<th>IGLOO</th>
<th>IGLOOE</th>
<th>IGLOO Plus</th>
<th>ProASIC3</th>
<th>ProASIC3E</th>
<th>ProASIC3L</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash*Freeze Mode</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Typical Quiescent Current</td>
<td>1.9uA</td>
<td>600uA</td>
<td>4uA</td>
<td>34uA</td>
<td>4uA</td>
<td>2mA</td>
<td>5mA</td>
<td>0.33mA</td>
</tr>
<tr>
<td>Static Power</td>
<td>2uW</td>
<td>0.9mW</td>
<td>5uW</td>
<td>40.8uW</td>
<td>5uW</td>
<td>3mW</td>
<td>7.5mW</td>
<td>0.4mW</td>
</tr>
</tbody>
</table>

- IGLOO nano offers industry’s lowest power
- IGLOO family offers Flash*Freeze mode to obtain low static currents
- Flash*Freeze mode
  - Enter and exit ultra-low power mode using single pin control
  - Retains SRAM content and register data
Flash FPGA Heritage

- Used in many safety-critical and mission-critical applications

<table>
<thead>
<tr>
<th>Space</th>
<th>Aviation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ExoMars TGO</strong></td>
<td><strong>Boeing 787</strong></td>
</tr>
<tr>
<td><img src="image1" alt="ExoMars TGO" /></td>
<td><img src="image2" alt="Boeing 787" /></td>
</tr>
<tr>
<td><strong>LADEE</strong></td>
<td><strong>Airbus A400M</strong></td>
</tr>
<tr>
<td><img src="image3" alt="LADEE" /></td>
<td><img src="image4" alt="Airbus A400M" /></td>
</tr>
<tr>
<td><strong>IRIS</strong></td>
<td><strong>F-35 JSF</strong></td>
</tr>
<tr>
<td><img src="image5" alt="IRIS" /></td>
<td><img src="image6" alt="F-35 JSF" /></td>
</tr>
<tr>
<td><strong>Orbcomm G2</strong></td>
<td><strong>Airbus A350</strong></td>
</tr>
<tr>
<td><img src="image7" alt="Orbcomm G2" /></td>
<td><img src="image8" alt="Airbus A350" /></td>
</tr>
</tbody>
</table>
Microsemi continues to innovate new non-volatile FPGA technologies

- Highest reliability
- Radiation configuration upset immunity
- Lowest power consumption
Conclusion

- CMOS FIT Rate based on HTOL data (cumulative) < 10 FIT for three most recent generations of Microsemi Flash FPGAs
  - The calculated FIT is based on 60% confidence level @ 55°C using $E_a = 0.7 \text{eV}$

- Several device-package combinations are available with hermetically sealed ceramic packages and QML class Q or MIL-STD-883 class B screening

- Many more device-package combinations are available with plastic packaging and military temperature screening

- Reliability Studies performed to date did not reveal any potential issues with four generations of Flash FPGA

- Microsemi will continue its commitment to the Defense and Aerospace industries by delivering FPGAs with proven reliability and advanced features
Contact Information

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