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# Micro-machined High Density Embedded Capacitor Technologies for Energy Storage Applications

by

Thomas A. Baginski , Robert N. Dean, Michael Hamilton, John J. Tatarchuk  
and Aubrey N. Beal

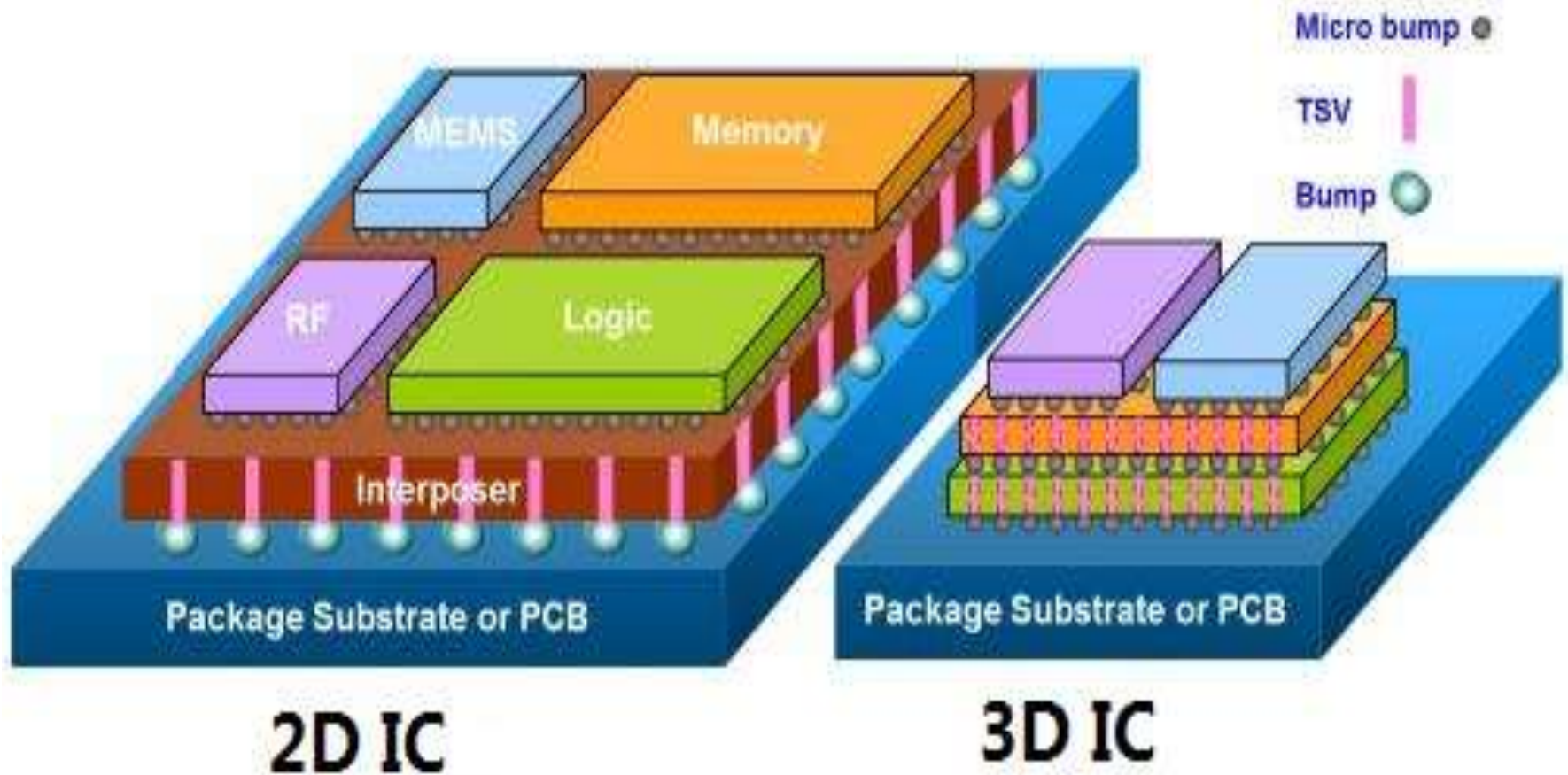
Auburn University, Auburn AL

# MEMS Super Capacitors: Application

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- Substrate embeddable to provide current to circuits during power anomaly (i.e. Interposer)
- Requires low inductance path for rapid current discharge
- Requires etched cavities to increase surface area of capacitor

# Interposer Provides Power Source Directly to Chips



# Approach and Concepts

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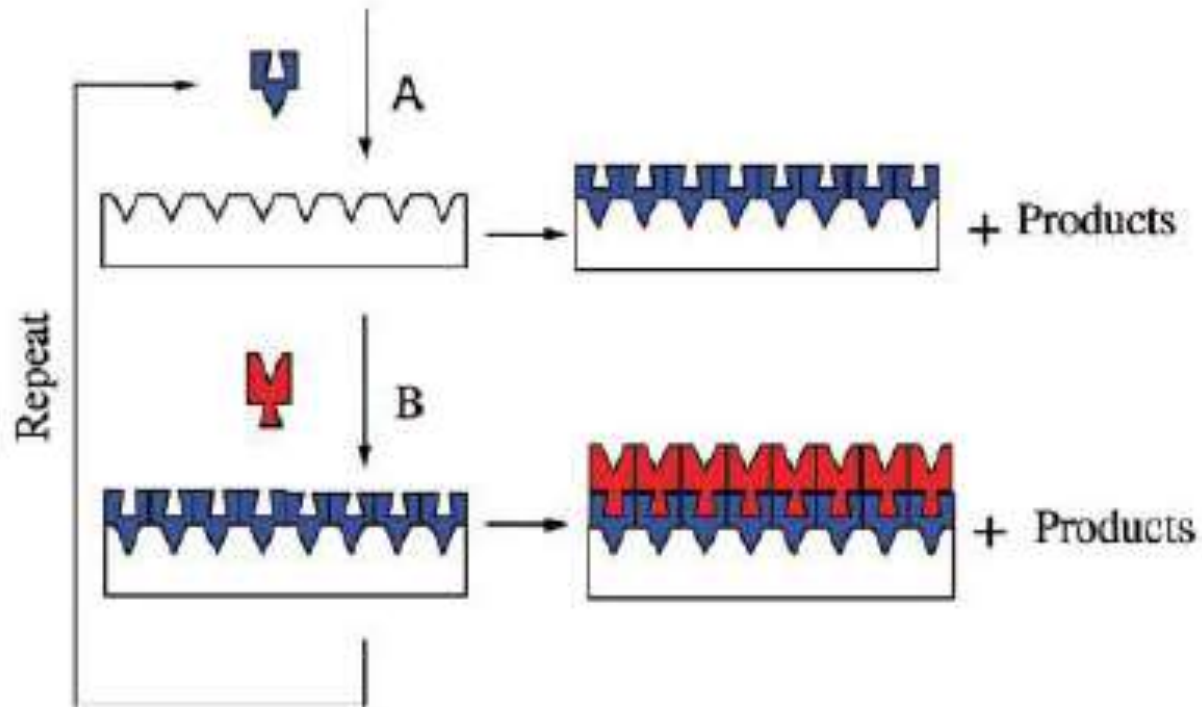
- Fabricate Planar Structure with  $\text{SiO}_2$  (relative permittivity ~ 3.8)
- Fabricate Planar Structure with Atomic Level Deposition (ALD)  $\text{HfO}_2$  (large relative permittivity ~ 25) from multiple vendors
- Fabricate Planar Structure with ALD  $\text{HfO}_2$  and DRIE etched features
- Characterize Discharge Characteristics
- Summary

# MEMS Super Capacitors: Fabrication

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- n-type <100> silicon wafers
- Oxidized in steam/dry O<sub>2</sub> @ 1050° C for 1- 4 hours      0.15μm < t<sub>ox</sub> < 0.8μm
- Top side selectively DRIE etched (increase surface area) and selectively doped
- Atomic Level Deposition performed
- Metalized with 100nm Ti /0.4μm of Cu

# Basic Atomic Level Deposition Process



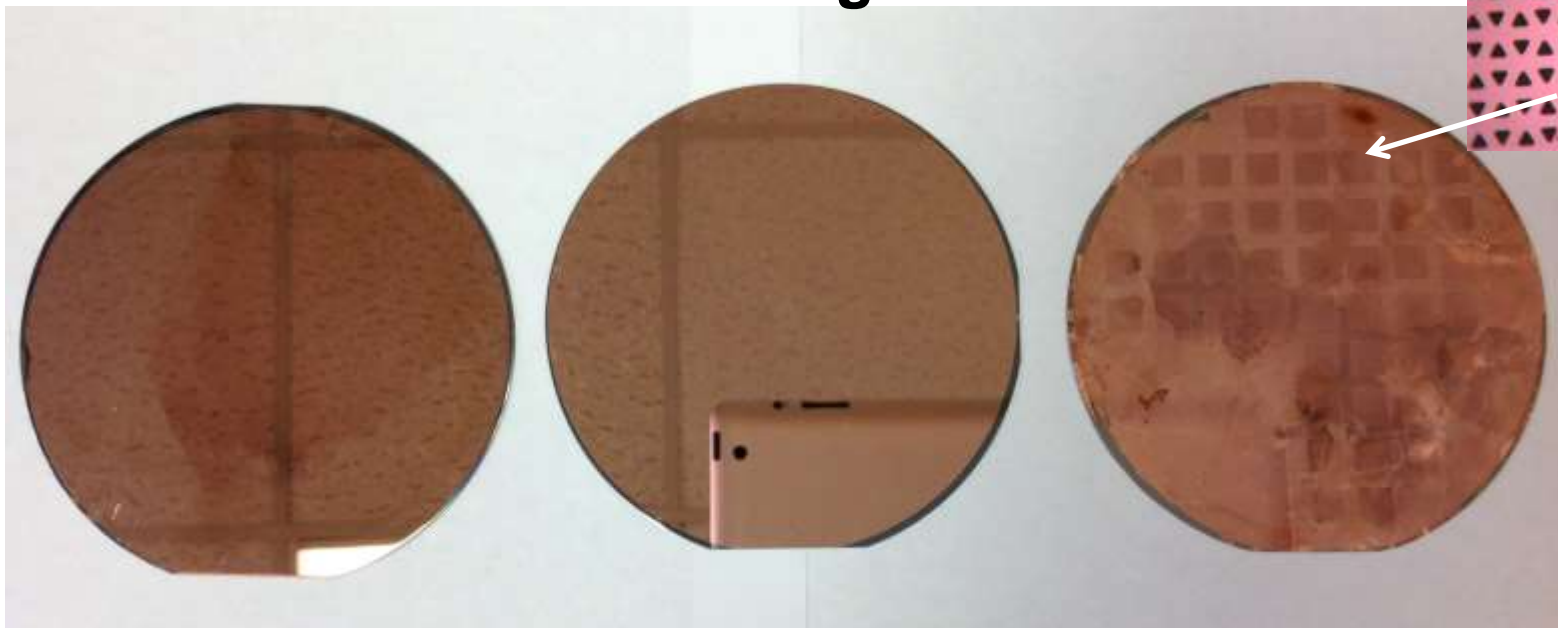
# Interposer Capacitor 100 mm Silicon Test Wafers

Thermal  $\text{SiO}_2$

ALD  $\text{HfO}_2$   
GIT

ALD  $\text{HfO}_2$   
Cam. Nano.

All Samples Initially Charged to 2V and then Discharged



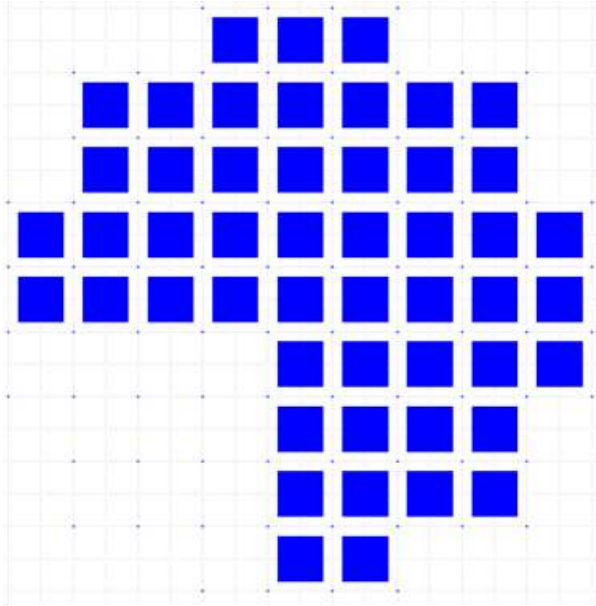
800nm

3nm & 10nm

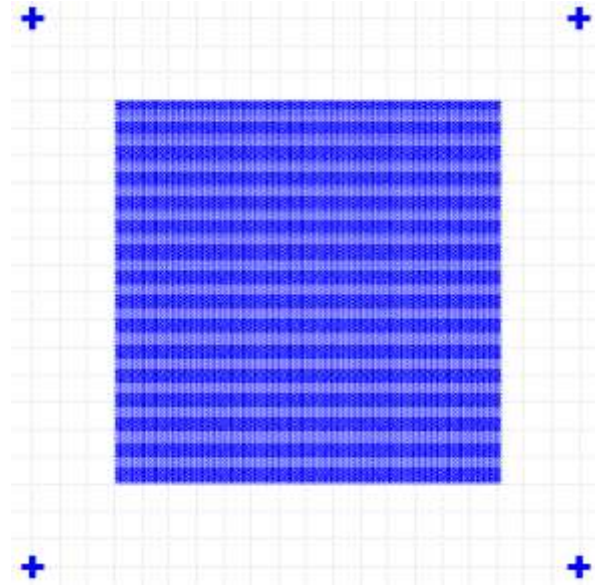
30nm

# MEMS Super Capacitors: Micromachining Pattern

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Layout of Wafer

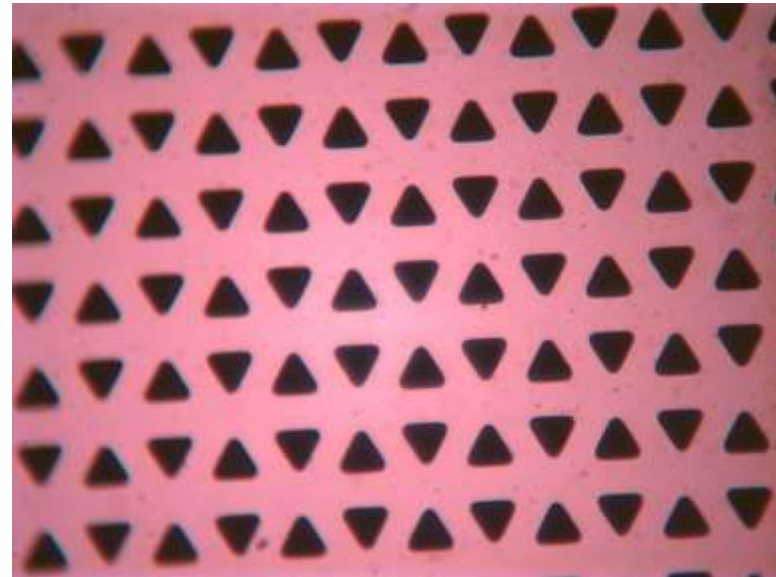
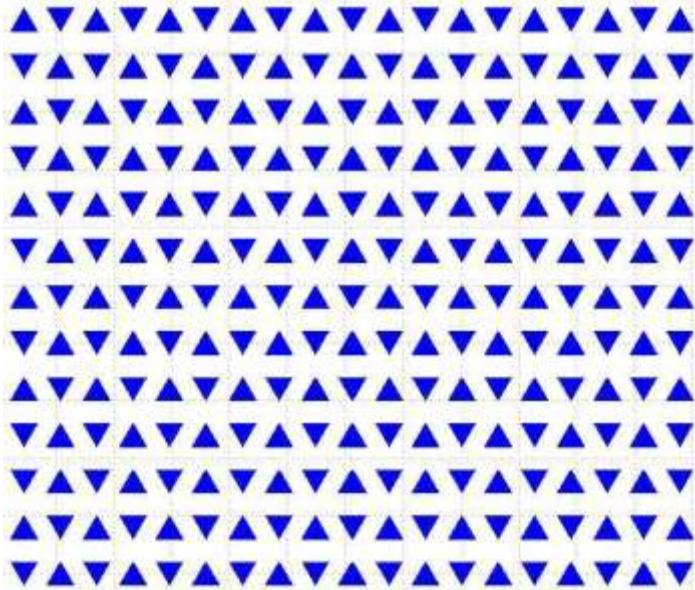


Layout of Individual Chip

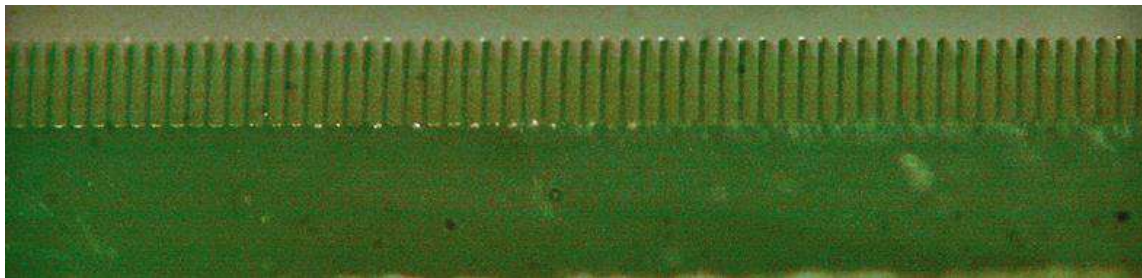
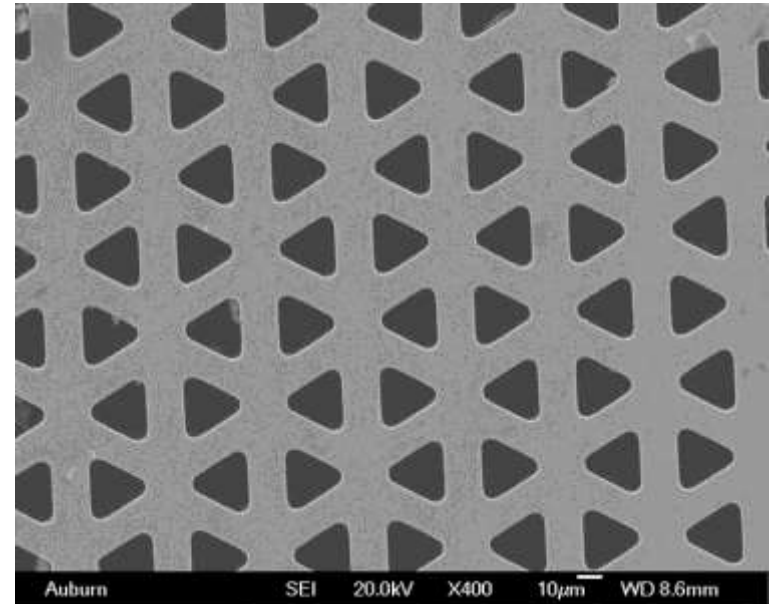
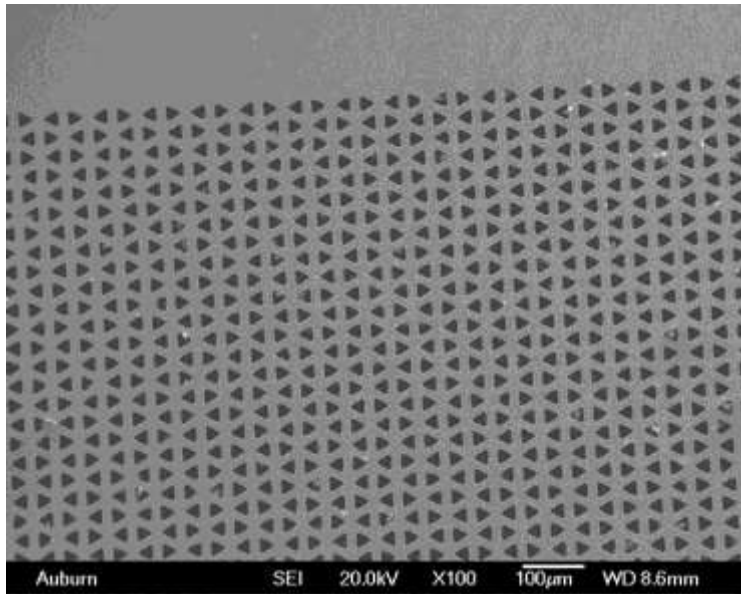


# Cylinder and Triangle Pattern Utilized

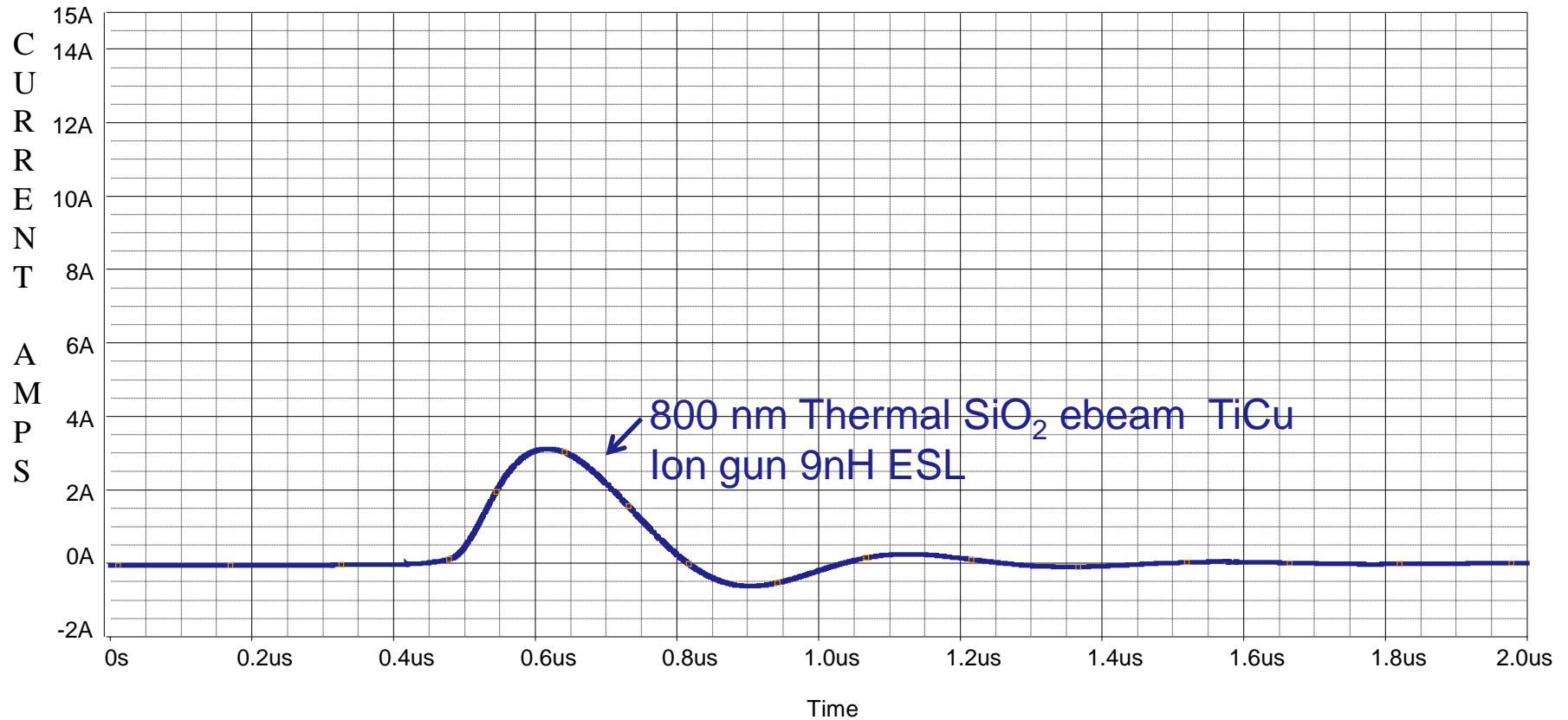
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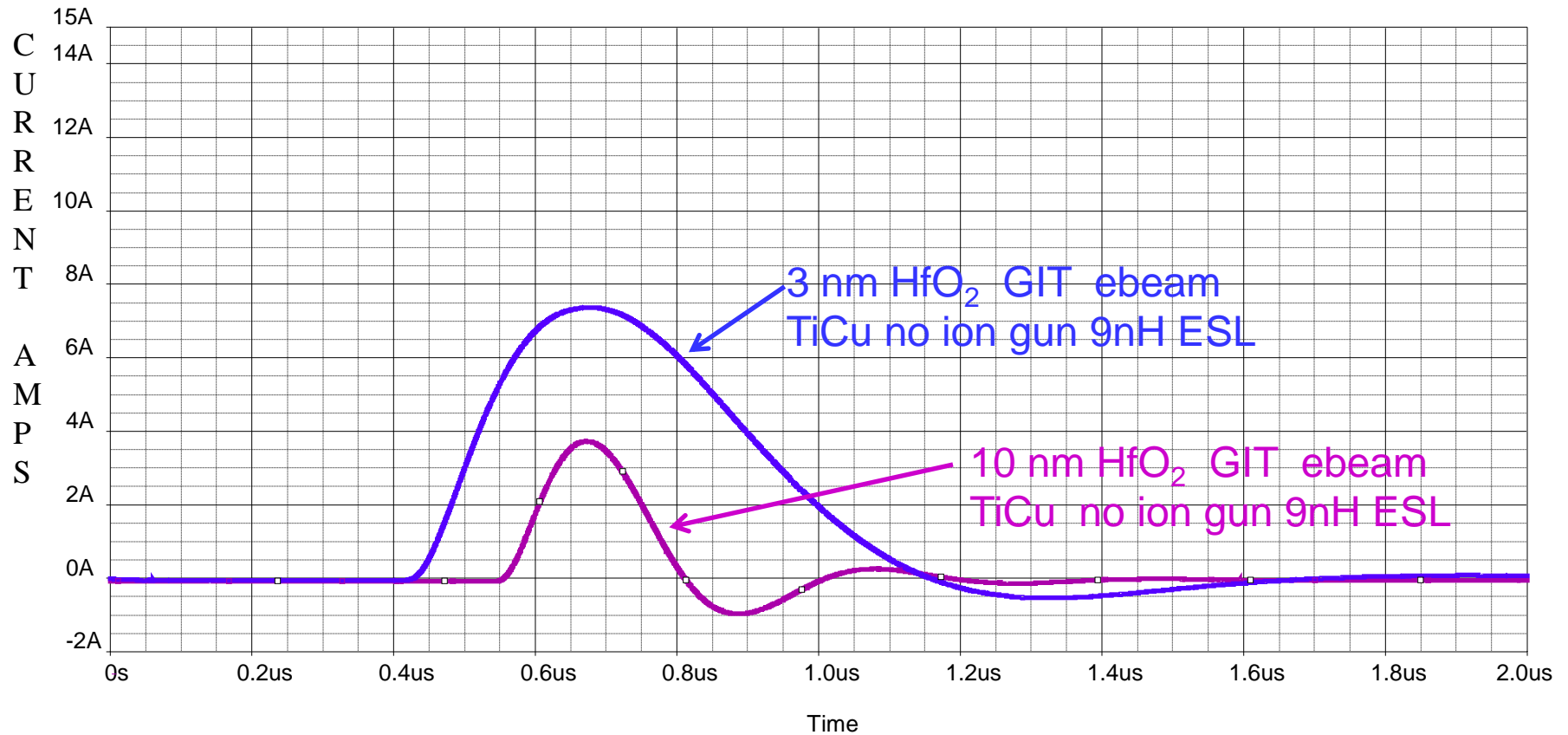
# SEM & Photo Micrographs of DRIE Etched Features



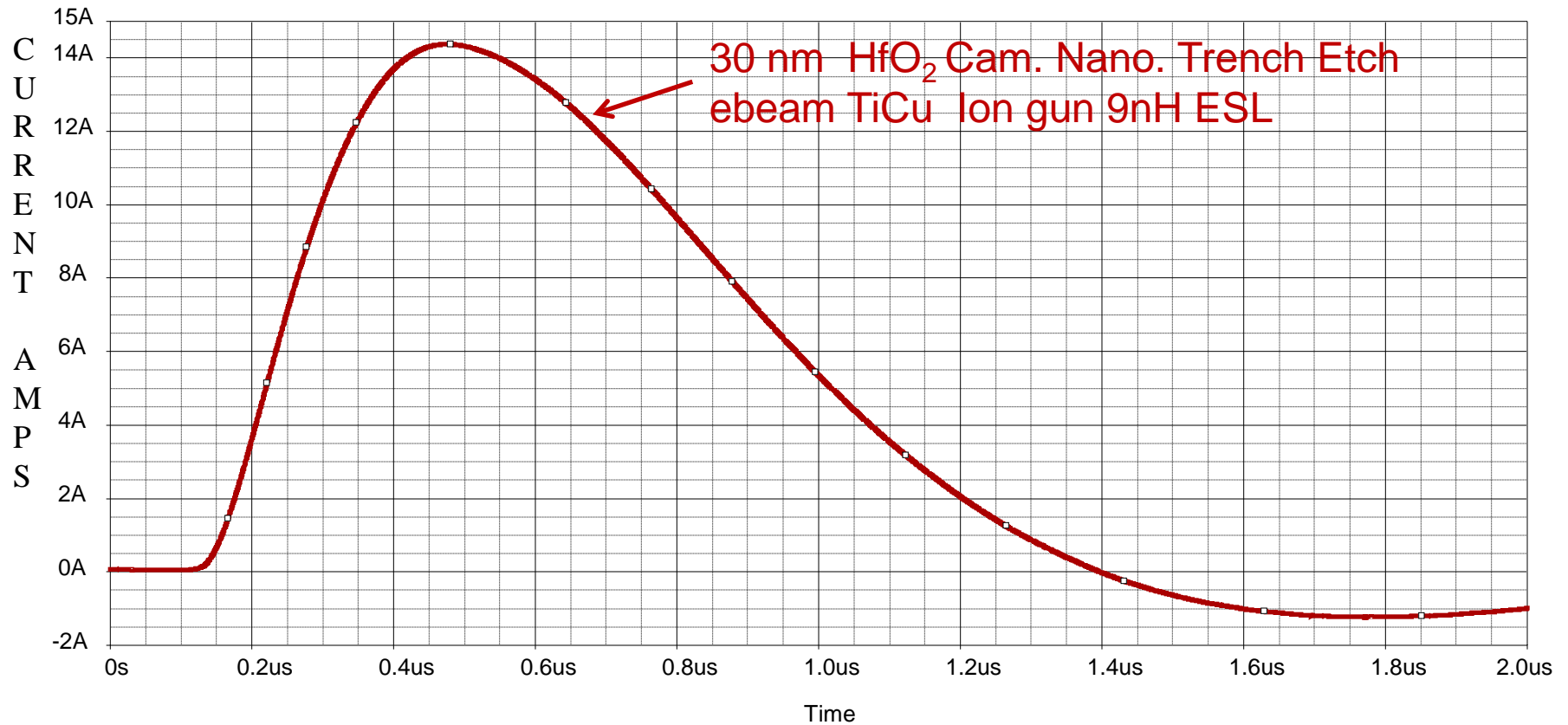
# Thermal SiO<sub>2</sub> E-beam TiCu



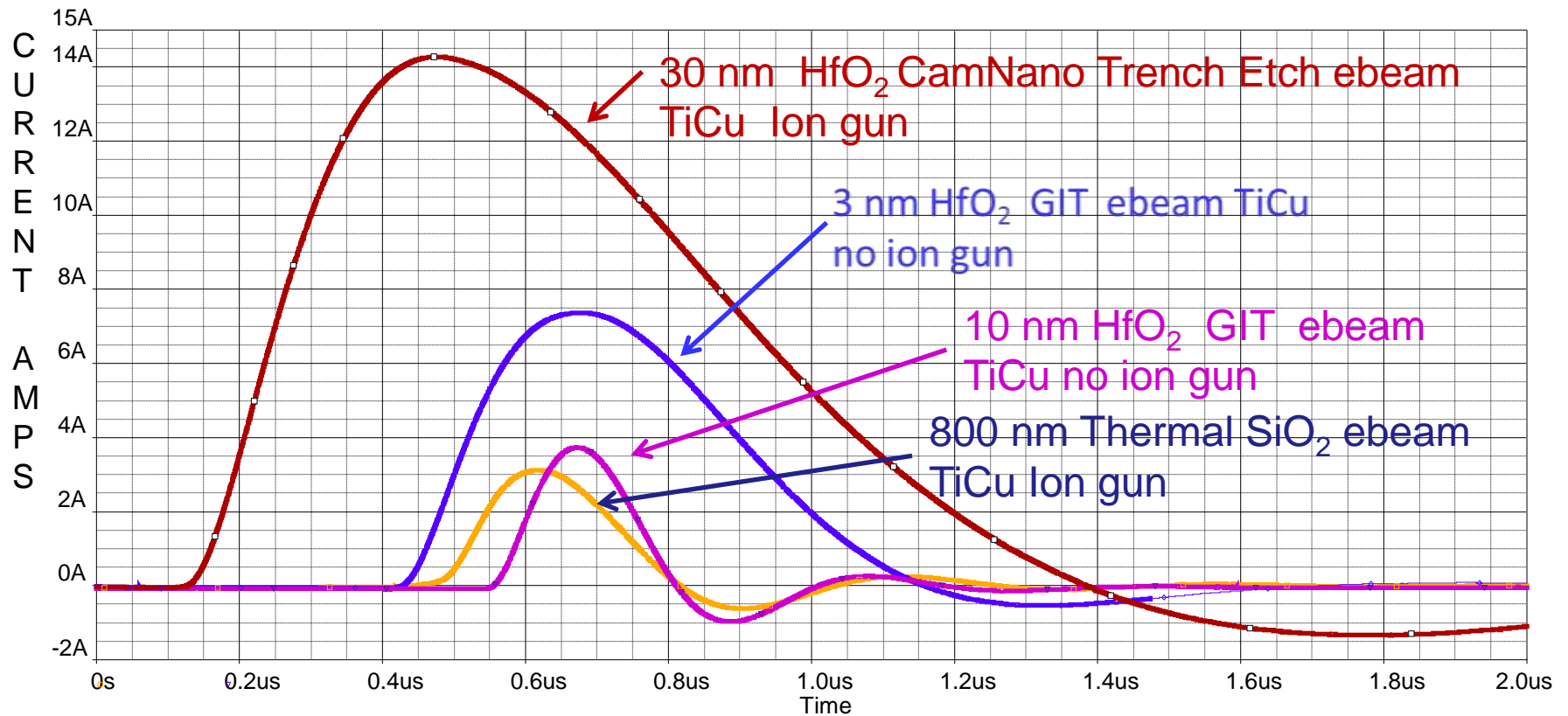
# ALD HfO<sub>2</sub> GIT E-beam TiCu



# ALD HfO<sub>2</sub> Cam. Nano. E-beam TiCu



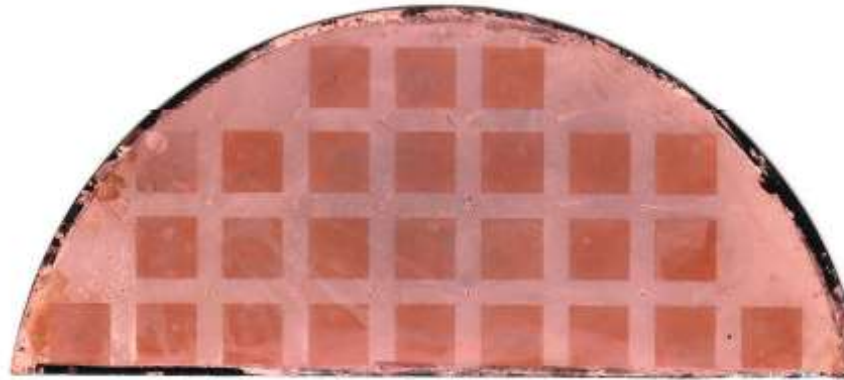
# Composite



# Half Wafer HfO<sub>2</sub> Capacitor

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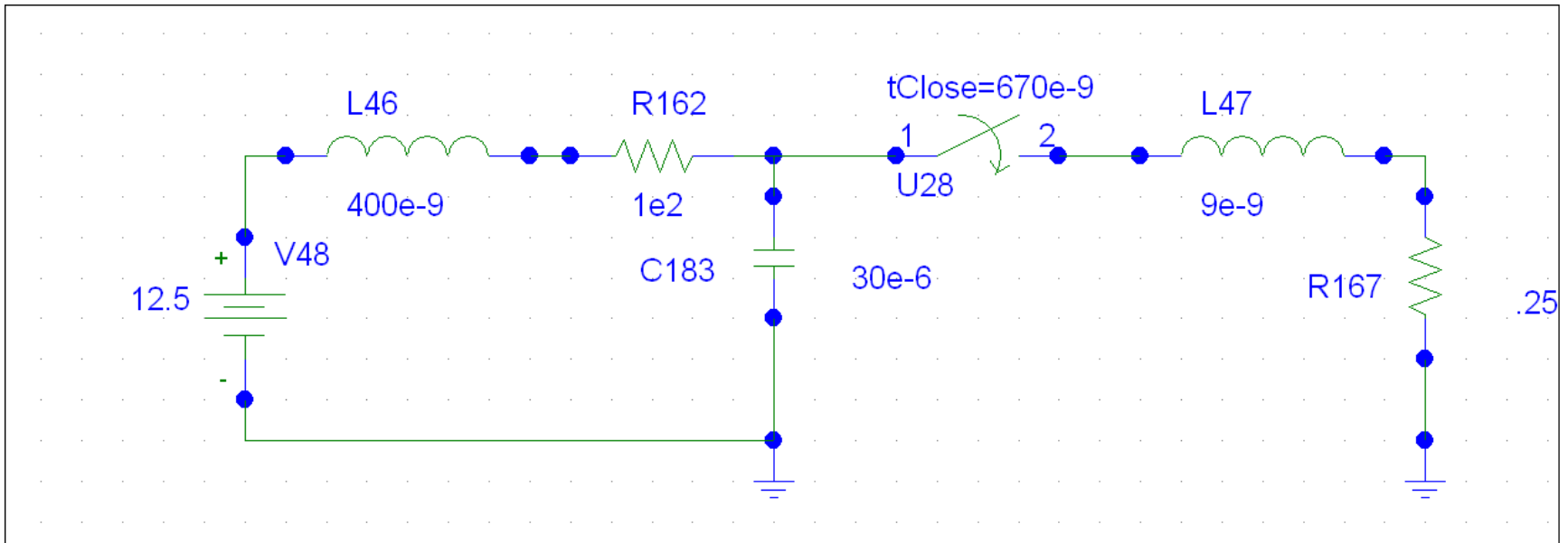
Sample Charged to 12.5V and then Discharged



$$C = (\epsilon_R \epsilon_0 \text{Area}) / t_o$$

$$C \sim 30,000\text{nF}$$

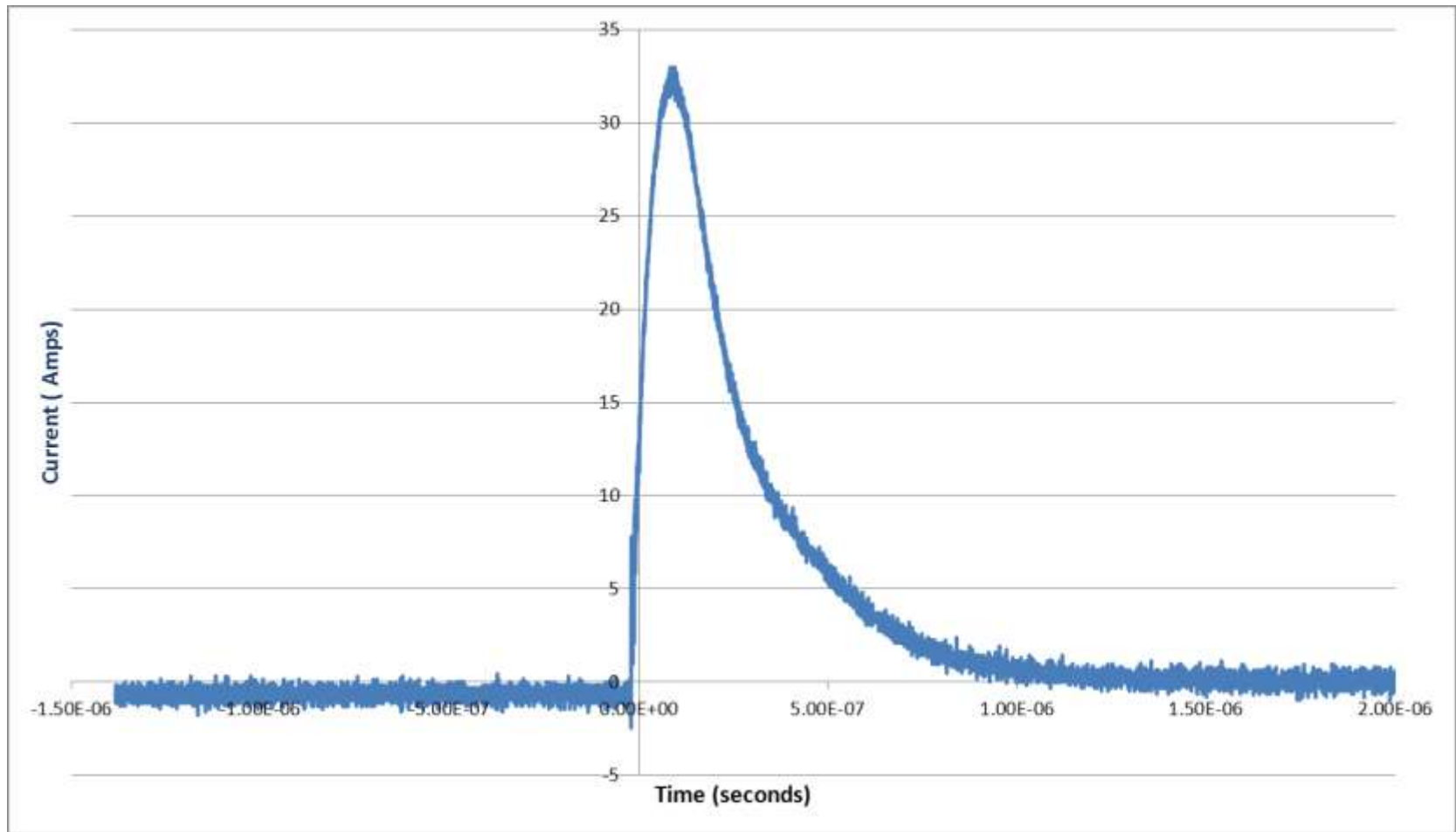
# Test Circuit for Half Wafer HfO<sub>2</sub> Capacitor: 9nH ESL





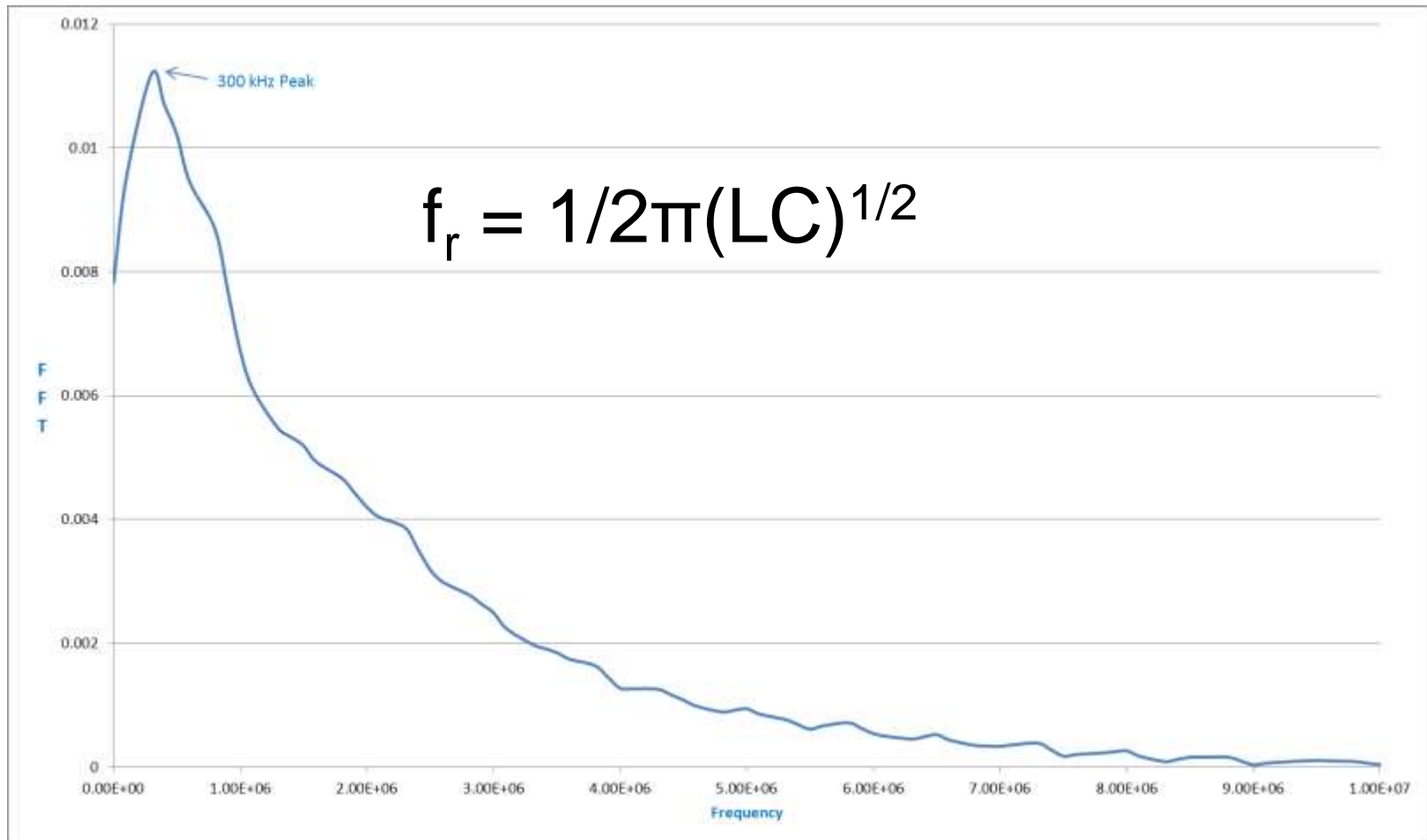
# Ringdown in Time Domain

- 30nm thick hafnium oxide 30,000nF 12.5V discharge with an ESL = 9nH  
ESR = 0.25Ω



# FFT of Ringdown

- 30nm thick hafnium oxide 30,000nF 12.5V discharge with an ESL = 9nH  
ESR = 0.25Ω



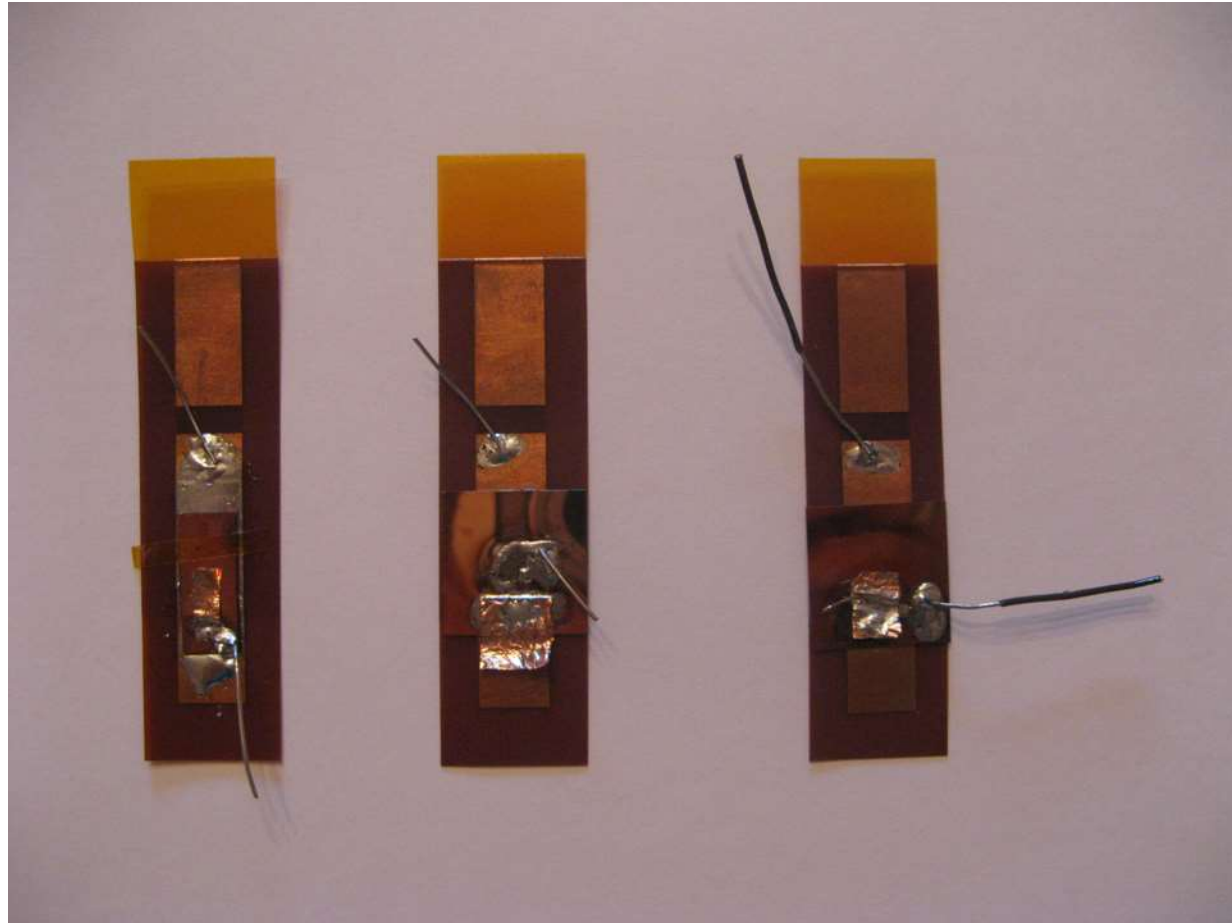
# MEMS Super Capacitors: SPICE Modeling

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- High speed ringdown tests for a variety of configurations performed to determine capacitor performance under rapid discharge conditions
- Empirical data compared graphically to theoretical voltage discharge profiles
- Current discharge calculated from  $C(dV/dt)$
- Results plotted and compared

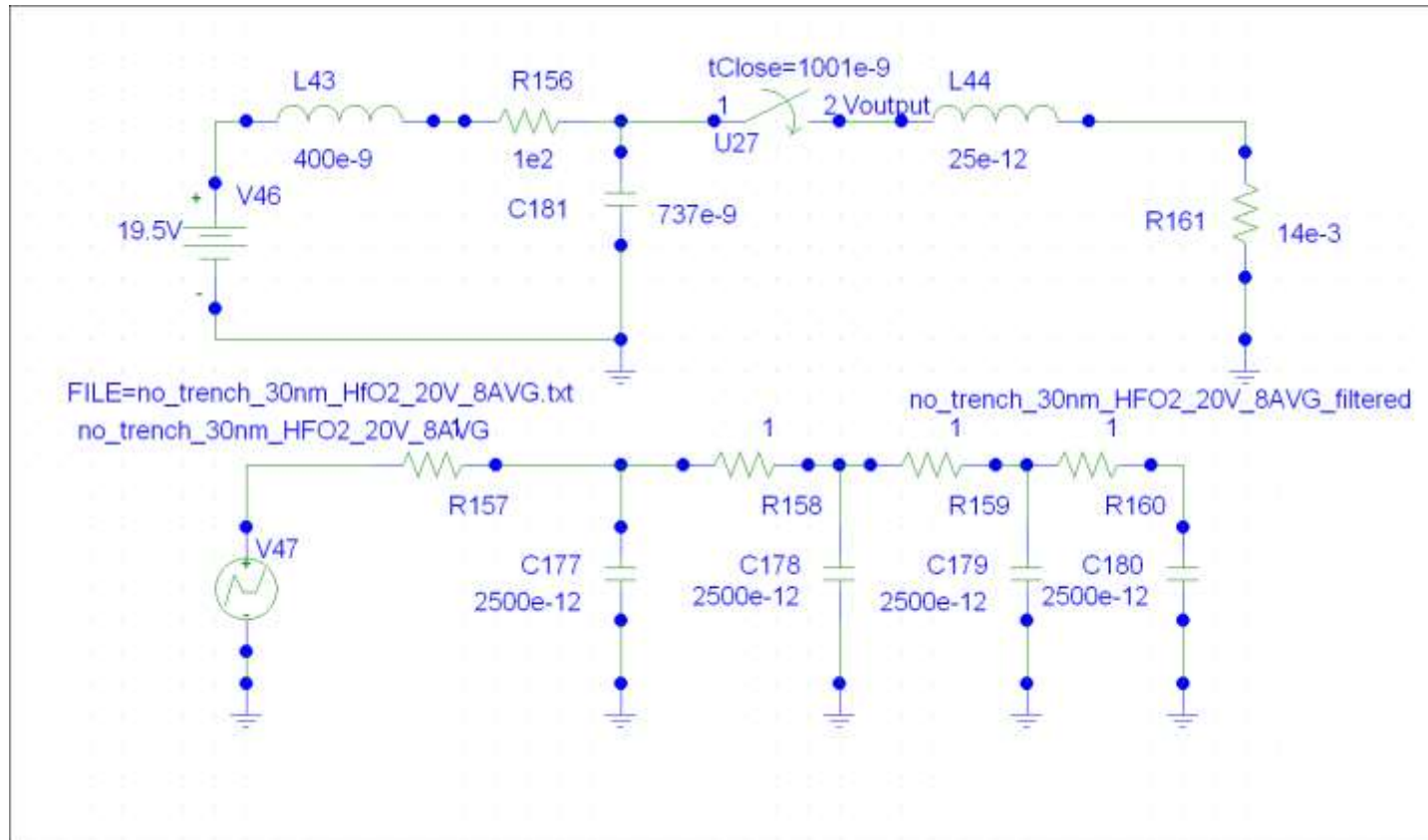
# MEMS Super Capacitors: Photos

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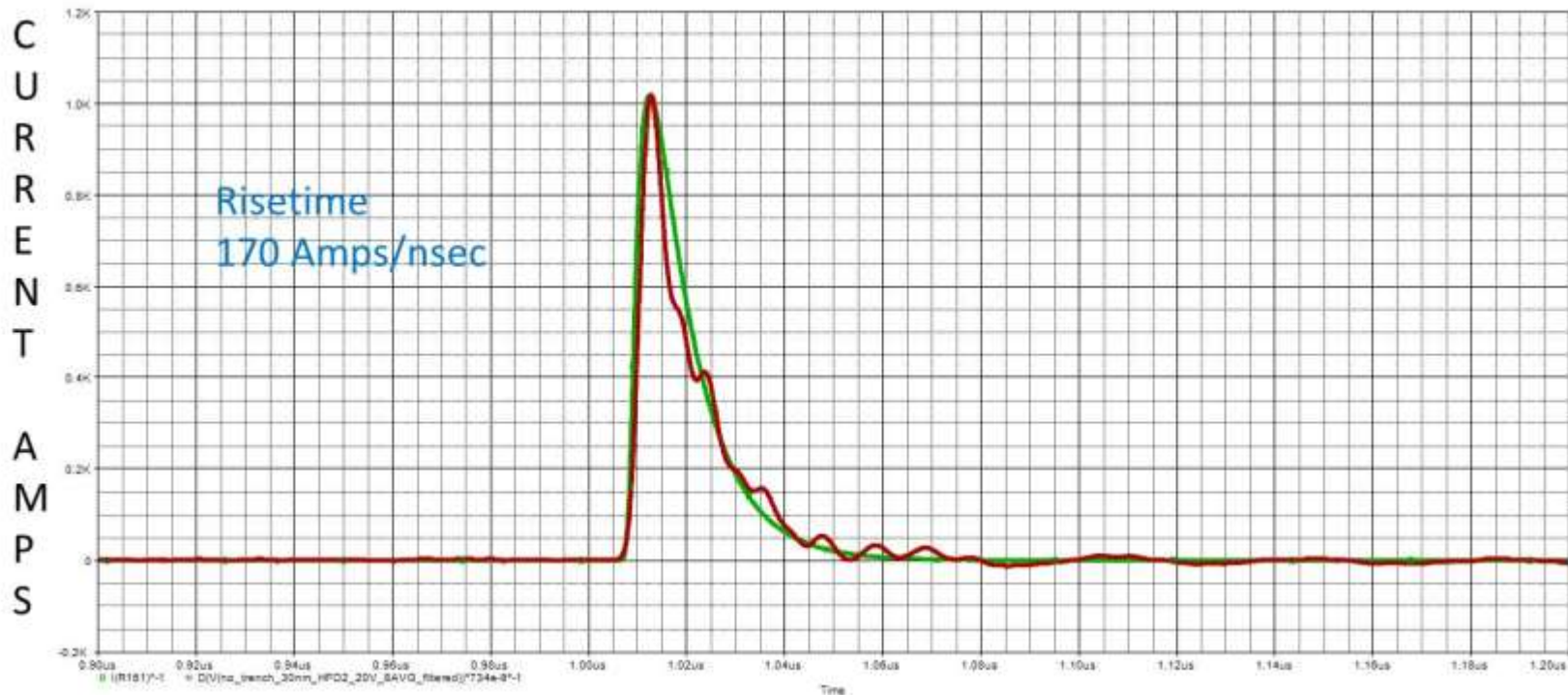
# PSPICE Model

- 30nm thick hafnium oxide capacitor  $C = 734\text{nF}$ ,  
19.5V discharge voltage with an  $\text{ESL} = 25\text{pH}$   $\text{ESR} = 14\text{m}\Omega$



# Ringdown in Time Domain

- 30nm thick hafnium oxide capacitor  $C = 734\text{nF}$ ,  
19.5V discharge voltage with an ESL = 25pH ESR =  
14m $\Omega$



# Summary

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- Possible to fabricate high value capacitors for interposer
- Risetime dependent upon load
- $\text{HfO}_2$  has high dielectric constant ( $\sim 25$ )
- $\text{SiO}_2$  is more readily available from silicon foundries