Developing Systems Engineering Processes from Existing Software Processes

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Electronic Systems Laboratory
Georgia Tech Research Institute
Georgia Institute of Technology
Georgia Tech Research Institute (GTRI) Overview

- Unit of the Georgia Institute of Technology
- 1200+ employees
- 70% of research employees hold advanced degrees
- Wide variety of products
- Customers include federal and state government; and industry
- Competitively bid projects range greatly in size and duration
Overview

Transitional to Systems Engineering
Configuration Management
Project Planning
Peer Reviews
Summary
Questions
Systems Engineering

- Mechanical
- Electrical
- Optical
- Software
- Structural

System

Circuit Card
Starting Point

- Software developers were using CMM level 3 development processes
- An increasing number of programs included hardware components
- Developers with SW and HW expertise were informally carrying some processes to HW development
- Hired additional QA/Process Engineer with hardware development experience
HW Development Process Overview
Beginning the Transition

- Removed “software” from our documented processes and procedures where appropriate
- Discovered that many existing procedures mapped reasonably well to Systems Engineering
- Identified additional items for project planning and peer reviews
- Configuration management did not map well at the lower-level details
Work Products by Phase - Planning
Work Products by Phase - Requirements
Work Products by Phase - Design

Design Document
Work Products by Phase - Implementation

Circuit Card Assembly

Printed Wire Board

Layout
Work Products by Phase – Integration and Test
CM Issues: What to Control?

- Many new types of configuration items are introduced with hardware
- Developers need guidance in what to control – important interim CIs are often overlooked
CM Issues: New CIs to Control

- Gerbers
- VHDL
- Netlists
- Schematics
- Cable Drawings
- BOM / Parts List
- Data Sheets
- Symbol Libraries
- Technical Data Packages
- Assembly Drawings
- Text Fixtures / Test Code
- Master Pattern Drawings
CM Issues: Don’t lose Control

- Remember to control all files associated with HW development

- Items being fabricated (internally or externally) must be put under configuration control in advance

- Maintain control of physical HW items – which version of the card, firmware, embedded SW, and wire-mods are on the card

- Work products documented using multiple configuration items must be baselined

- Beware of “back-of-the-envelope” and red-line issues in fabrication
Example Directory Structure

System
  CCA-1
    SW
    HW
      Assembly
      Datasheets
      Development Folder
      Documents
      Gerbers
      Plans
      PLDs
      Schematics

CCA-2
CCA-N
# File Types

<table>
<thead>
<tr>
<th>Schematics</th>
<th>Gerbers</th>
<th>PLDs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet 1</td>
<td>Layer 1</td>
<td>FPGA</td>
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<tr>
<td>Sheet N</td>
<td>:</td>
<td>VHDL</td>
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<tr>
<td>Netlist</td>
<td>:</td>
<td>CPLD</td>
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<tr>
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<td>.ipc Test File</td>
<td>VHDL</td>
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<tr>
<td>Symbol Library</td>
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<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Mechanical Outline</td>
<td></td>
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<tr>
<td>Assembly Drawing</td>
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<tr>
<td>Master Pattern Drawing</td>
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<td></td>
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<tr>
<td>BOM / Parts List</td>
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</tbody>
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- **File Types**
  - **Schematics**
    - Sheet 1
    - Sheet N
    - Netlist
    - Symbol Library
  - **Assembly**
    - Mechanical Outline
    - Assembly Drawing
    - Master Pattern Drawing
    - BOM / Parts List
  - **Gerbers**
    - Layer 1
    - Layer N
    - .ipc Test File
  - **PLDs**
    - FPGA
    - VHDL
    - CPLD
    - VHDL
## File Types – Continued

<table>
<thead>
<tr>
<th>Documents</th>
<th>Plans</th>
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<tr>
<td>Requirements</td>
<td>CM Plan</td>
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<tr>
<td>Design Description</td>
<td>Project Plan</td>
</tr>
<tr>
<td>Interface Control Document</td>
<td>HW Development Plan</td>
</tr>
<tr>
<td>Baseline Documents</td>
<td>Test Plan</td>
</tr>
<tr>
<td>Test Descriptions</td>
<td></td>
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<tr>
<td>Product Version Description</td>
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</tr>
<tr>
<td>Development Folder</td>
<td>Data Sheets</td>
</tr>
<tr>
<td>Test scripts</td>
<td>Parts vendor info</td>
</tr>
</tbody>
</table>

- **Files in Documents**:
  - Requirements
  - Design Description
  - Interface Control Document
  - Baseline Documents
  - Test Descriptions
  - Product Version Description

- **Files in Plans**:
  - CM Plan
  - Project Plan
  - HW Development Plan
  - Test Plan

- **Files in Development Folder**:
  - Test scripts

- **Files in Data Sheets**:
  - Parts vendor info
Project Planning Issues

• Long lead times / critical path
• Facilities and equipment management
• Developmental baselines needed for fabrication
• “Hidden” software items
Peer Review Issues

- Consider schedule impact as well as cost-effectiveness
- Proper baselining of reviewed materials with multiple configuration items
- VHDL (Very High-speed Integrated Circuit Hardware Description Language) is software!
Peer Review Issues

• Review hardware configuration items such as Gerber files, drawing packages (schematics, wiring diagrams, assembly drawings, parts lists, mechanical part designs, etc.)

• Select reviewers with HW and SW knowledge – be aware of software denial

• Review test software needed to exercise hardware
Beware

- Software “hiding” inside hardware items
- Tracing hardware requirements to hardware design
- Fabrication from uncontrolled designs
- “Quick fixes” that don’t get documented
- Changing HW configurations
- Software needed for HW testing
Acronyms

- BOM – Bill of Materials
- CCA – Circuit Card Assembly
- CI – Configuration Items
- CMM – Capability Maturity Model
- CMMI – Capability Maturity Model Integration
- GTRI – Georgia Tech Research Institute
- HW – Hardware
- PLD – Programmable Logic Device
- SW – Software
- VHDL – Very High-speed Integrated Circuit Hardware Description Language
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